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# Static Timing Analysis

|  |  |
| --- | --- |
| **Project :** | IDAC8\_Example01 |
| **Build Time :** | 08/19/19 18:32:45 |
| **Device :** | CY8C5888LTI-LP097 |
| **Temperature :** | -40C - 85/125C |
| **VDDA :** | 5.00 |
| **VDDABUF :** | 5.00 |
| **VDDD :** | 5.00 |
| **VDDIO0 :** | 5.00 |
| **VDDIO1 :** | 5.00 |
| **VDDIO2 :** | 5.00 |
| **VDDIO3 :** | 5.00 |
| **VUSB :** | 5.00 |
| **Voltage :** | 5.0 |

[Expand All](#gjdgxs) | [Collapse All](#gjdgxs) | [Show All Paths](#gjdgxs) | [Hide All Paths](#gjdgxs)

[**+ Timing Violation Section**](#gjdgxs)

No Timing Violations

[**+ Clock Summary Section**](#gjdgxs)

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Clock | Domain | Nominal Frequency | Required Frequency | Maximum Frequency | Violation |
| ADC\_DelSig\_1\_Ext\_CP\_Clk | ADC\_DelSig\_1\_Ext\_CP\_Clk | 24.000 MHz | 24.000 MHz | N/A |  |
| ADC\_DelSig\_1\_Ext\_CP\_Clk(routed) | ADC\_DelSig\_1\_Ext\_CP\_Clk(routed) | 24.000 MHz | 24.000 MHz | N/A |  |
| ClockBlock/aclk\_glb\_ff\_0 | ClockBlock/aclk\_glb\_ff\_0 | UNKNOWN | UNKNOWN | N/A |  |
| CyILO | CyILO | 1.000 kHz | 1.000 kHz | N/A |  |
| CyIMO | CyIMO | 3.000 MHz | 3.000 MHz | N/A |  |
| CyMASTER\_CLK | CyMASTER\_CLK | 24.000 MHz | 24.000 MHz | N/A |  |
| CyBUS\_CLK | CyMASTER\_CLK | 24.000 MHz | 24.000 MHz | 56.792 MHz |  |
| ADC\_DelSig\_1\_theACLK | CyMASTER\_CLK | 631.579 kHz | 631.579 kHz | N/A |  |
| UART\_1\_IntClock | CyMASTER\_CLK | 461.538 kHz | 461.538 kHz | 51.722 MHz |  |
| CyPLL\_OUT | CyPLL\_OUT | 24.000 MHz | 24.000 MHz | N/A |  |
| \ADC\_DelSig\_1:DSM\/dec\_clock | \ADC\_DelSig\_1:DSM\/dec\_clock | UNKNOWN | UNKNOWN | N/A |  |

[**+ Register to Register Section**](#gjdgxs)

[**+ Setup Subsection**](#gjdgxs)

[**+ Source Clock : CyBUS\_CLK : Positive edge(Required Frequency 24 MHz)**](#gjdgxs)

[**+ Destination Clock : UART\_1\_IntClock : Positive edge(Required Frequency 461.538 kHz)**](#gjdgxs)

Path Delay Requirement : 41.6667ns(24 MHz)

Affects clock : CyMASTER\_CLK

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Source | Destination | FMax | Delay (ns) | Slack (ns) | Violation |
| Rx\_1(0)/fb | \UART\_1:BUART:sRX:RxShifter:u0\/route\_si | 56.792 MHz | 17.608 | 24.059 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | iocell2 | P0[0] | 1 | Rx\_1(0) | Rx\_1(0)/in\_clock | Rx\_1(0)/fb | 2.183 | | Route |  | 1 | Net\_188 | Rx\_1(0)/fb | \UART\_1:BUART:rx\_postpoll\/main\_1 | 6.296 | | macrocell6 | U(3,5) | 1 | \UART\_1:BUART:rx\_postpoll\ | \UART\_1:BUART:rx\_postpoll\/main\_1 | \UART\_1:BUART:rx\_postpoll\/q | 3.350 | | Route |  | 1 | \UART\_1:BUART:rx\_postpoll\ | \UART\_1:BUART:rx\_postpoll\/q | \UART\_1:BUART:sRX:RxShifter:u0\/route\_si | 2.309 | | datapathcell3 | U(3,5) | 1 | \UART\_1:BUART:sRX:RxShifter:u0\ |  | SETUP | 3.470 | | Clock |  |  |  |  | Skew | 0.000 | | | | | | |
| Rx\_1(0)/fb | \UART\_1:BUART:pollcount\_0\/main\_2 | 85.266 MHz | 11.728 | 29.939 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | iocell2 | P0[0] | 1 | Rx\_1(0) | Rx\_1(0)/in\_clock | Rx\_1(0)/fb | 2.183 | | Route |  | 1 | Net\_188 | Rx\_1(0)/fb | \UART\_1:BUART:pollcount\_0\/main\_2 | 6.035 | | macrocell23 | U(3,3) | 1 | \UART\_1:BUART:pollcount\_0\ |  | SETUP | 3.510 | | Clock |  |  |  |  | Skew | 0.000 | | | | | | |
| Rx\_1(0)/fb | \UART\_1:BUART:rx\_status\_3\/main\_6 | 85.266 MHz | 11.728 | 29.939 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | iocell2 | P0[0] | 1 | Rx\_1(0) | Rx\_1(0)/in\_clock | Rx\_1(0)/fb | 2.183 | | Route |  | 1 | Net\_188 | Rx\_1(0)/fb | \UART\_1:BUART:rx\_status\_3\/main\_6 | 6.035 | | macrocell24 | U(3,3) | 1 | \UART\_1:BUART:rx\_status\_3\ |  | SETUP | 3.510 | | Clock |  |  |  |  | Skew | 0.000 | | | | | | |
| Rx\_1(0)/fb | \UART\_1:BUART:rx\_last\/main\_0 | 85.266 MHz | 11.728 | 29.939 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | iocell2 | P0[0] | 1 | Rx\_1(0) | Rx\_1(0)/in\_clock | Rx\_1(0)/fb | 2.183 | | Route |  | 1 | Net\_188 | Rx\_1(0)/fb | \UART\_1:BUART:rx\_last\/main\_0 | 6.035 | | macrocell25 | U(3,3) | 1 | \UART\_1:BUART:rx\_last\ |  | SETUP | 3.510 | | Clock |  |  |  |  | Skew | 0.000 | | | | | | |
| Rx\_1(0)/fb | \UART\_1:BUART:rx\_state\_0\/main\_9 | 90.155 MHz | 11.092 | 30.575 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | iocell2 | P0[0] | 1 | Rx\_1(0) | Rx\_1(0)/in\_clock | Rx\_1(0)/fb | 2.183 | | Route |  | 1 | Net\_188 | Rx\_1(0)/fb | \UART\_1:BUART:rx\_state\_0\/main\_9 | 5.399 | | macrocell16 | U(3,4) | 1 | \UART\_1:BUART:rx\_state\_0\ |  | SETUP | 3.510 | | Clock |  |  |  |  | Skew | 0.000 | | | | | | |
| Rx\_1(0)/fb | \UART\_1:BUART:rx\_state\_2\/main\_8 | 90.155 MHz | 11.092 | 30.575 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | iocell2 | P0[0] | 1 | Rx\_1(0) | Rx\_1(0)/in\_clock | Rx\_1(0)/fb | 2.183 | | Route |  | 1 | Net\_188 | Rx\_1(0)/fb | \UART\_1:BUART:rx\_state\_2\/main\_8 | 5.399 | | macrocell19 | U(3,4) | 1 | \UART\_1:BUART:rx\_state\_2\ |  | SETUP | 3.510 | | Clock |  |  |  |  | Skew | 0.000 | | | | | | |
| Rx\_1(0)/fb | \UART\_1:BUART:pollcount\_1\/main\_3 | 90.310 MHz | 11.073 | 30.594 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | iocell2 | P0[0] | 1 | Rx\_1(0) | Rx\_1(0)/in\_clock | Rx\_1(0)/fb | 2.183 | | Route |  | 1 | Net\_188 | Rx\_1(0)/fb | \UART\_1:BUART:pollcount\_1\/main\_3 | 5.380 | | macrocell22 | U(3,4) | 1 | \UART\_1:BUART:pollcount\_1\ |  | SETUP | 3.510 | | Clock |  |  |  |  | Skew | 0.000 | | | | | | |

[**+ Source Clock : UART\_1\_IntClock : Positive edge(Required Frequency 461.538 kHz)**](#gjdgxs)

[**+ Destination Clock : UART\_1\_IntClock : Positive edge(Required Frequency 461.538 kHz)**](#gjdgxs)

Path Delay Requirement : 2166.67ns(461.538 kHz)

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Source | Destination | FMax | Delay (ns) | Slack (ns) | Violation |
| \UART\_1:BUART:tx\_state\_1\/q | \UART\_1:BUART:sTX:sCLOCK:TxBitClkGen\/cs\_addr\_0 | 51.722 MHz | 19.334 | 2147.333 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | macrocell11 | U(2,4) | 1 | \UART\_1:BUART:tx\_state\_1\ | \UART\_1:BUART:tx\_state\_1\/clock\_0 | \UART\_1:BUART:tx\_state\_1\/q | 1.250 | | Route |  | 1 | \UART\_1:BUART:tx\_state\_1\ | \UART\_1:BUART:tx\_state\_1\/q | \UART\_1:BUART:counter\_load\_not\/main\_0 | 6.250 | | macrocell2 | U(2,5) | 1 | \UART\_1:BUART:counter\_load\_not\ | \UART\_1:BUART:counter\_load\_not\/main\_0 | \UART\_1:BUART:counter\_load\_not\/q | 3.350 | | Route |  | 1 | \UART\_1:BUART:counter\_load\_not\ | \UART\_1:BUART:counter\_load\_not\/q | \UART\_1:BUART:sTX:sCLOCK:TxBitClkGen\/cs\_addr\_0 | 2.294 | | datapathcell2 | U(2,5) | 1 | \UART\_1:BUART:sTX:sCLOCK:TxBitClkGen\ |  | SETUP | 6.190 | | Clock |  |  |  |  | Skew | 0.000 | | | | | | |
| \UART\_1:BUART:tx\_state\_2\/q | \UART\_1:BUART:sTX:sCLOCK:TxBitClkGen\/cs\_addr\_0 | 54.357 MHz | 18.397 | 2148.270 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | macrocell13 | U(2,3) | 1 | \UART\_1:BUART:tx\_state\_2\ | \UART\_1:BUART:tx\_state\_2\/clock\_0 | \UART\_1:BUART:tx\_state\_2\/q | 1.250 | | Route |  | 1 | \UART\_1:BUART:tx\_state\_2\ | \UART\_1:BUART:tx\_state\_2\/q | \UART\_1:BUART:counter\_load\_not\/main\_3 | 5.313 | | macrocell2 | U(2,5) | 1 | \UART\_1:BUART:counter\_load\_not\ | \UART\_1:BUART:counter\_load\_not\/main\_3 | \UART\_1:BUART:counter\_load\_not\/q | 3.350 | | Route |  | 1 | \UART\_1:BUART:counter\_load\_not\ | \UART\_1:BUART:counter\_load\_not\/q | \UART\_1:BUART:sTX:sCLOCK:TxBitClkGen\/cs\_addr\_0 | 2.294 | | datapathcell2 | U(2,5) | 1 | \UART\_1:BUART:sTX:sCLOCK:TxBitClkGen\ |  | SETUP | 6.190 | | Clock |  |  |  |  | Skew | 0.000 | | | | | | |
| \UART\_1:BUART:tx\_state\_0\/q | \UART\_1:BUART:sTX:sCLOCK:TxBitClkGen\/cs\_addr\_0 | 59.552 MHz | 16.792 | 2149.875 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | macrocell12 | U(2,4) | 1 | \UART\_1:BUART:tx\_state\_0\ | \UART\_1:BUART:tx\_state\_0\/clock\_0 | \UART\_1:BUART:tx\_state\_0\/q | 1.250 | | Route |  | 1 | \UART\_1:BUART:tx\_state\_0\ | \UART\_1:BUART:tx\_state\_0\/q | \UART\_1:BUART:counter\_load\_not\/main\_1 | 3.708 | | macrocell2 | U(2,5) | 1 | \UART\_1:BUART:counter\_load\_not\ | \UART\_1:BUART:counter\_load\_not\/main\_1 | \UART\_1:BUART:counter\_load\_not\/q | 3.350 | | Route |  | 1 | \UART\_1:BUART:counter\_load\_not\ | \UART\_1:BUART:counter\_load\_not\/q | \UART\_1:BUART:sTX:sCLOCK:TxBitClkGen\/cs\_addr\_0 | 2.294 | | datapathcell2 | U(2,5) | 1 | \UART\_1:BUART:sTX:sCLOCK:TxBitClkGen\ |  | SETUP | 6.190 | | Clock |  |  |  |  | Skew | 0.000 | | | | | | |
| \UART\_1:BUART:rx\_state\_0\/q | \UART\_1:BUART:sRX:RxBitCounter\/load | 59.684 MHz | 16.755 | 2149.912 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | macrocell16 | U(3,4) | 1 | \UART\_1:BUART:rx\_state\_0\ | \UART\_1:BUART:rx\_state\_0\/clock\_0 | \UART\_1:BUART:rx\_state\_0\/q | 1.250 | | Route |  | 1 | \UART\_1:BUART:rx\_state\_0\ | \UART\_1:BUART:rx\_state\_0\/q | \UART\_1:BUART:rx\_counter\_load\/main\_1 | 4.488 | | macrocell5 | U(3,5) | 1 | \UART\_1:BUART:rx\_counter\_load\ | \UART\_1:BUART:rx\_counter\_load\/main\_1 | \UART\_1:BUART:rx\_counter\_load\/q | 3.350 | | Route |  | 1 | \UART\_1:BUART:rx\_counter\_load\ | \UART\_1:BUART:rx\_counter\_load\/q | \UART\_1:BUART:sRX:RxBitCounter\/load | 2.307 | | count7cell | U(3,5) | 1 | \UART\_1:BUART:sRX:RxBitCounter\ |  | SETUP | 5.360 | | Clock |  |  |  |  | Skew | 0.000 | | | | | | |
| \UART\_1:BUART:rx\_state\_2\/q | \UART\_1:BUART:sRX:RxBitCounter\/load | 59.913 MHz | 16.691 | 2149.976 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | macrocell19 | U(3,4) | 1 | \UART\_1:BUART:rx\_state\_2\ | \UART\_1:BUART:rx\_state\_2\/clock\_0 | \UART\_1:BUART:rx\_state\_2\/q | 1.250 | | Route |  | 1 | \UART\_1:BUART:rx\_state\_2\ | \UART\_1:BUART:rx\_state\_2\/q | \UART\_1:BUART:rx\_counter\_load\/main\_3 | 4.424 | | macrocell5 | U(3,5) | 1 | \UART\_1:BUART:rx\_counter\_load\ | \UART\_1:BUART:rx\_counter\_load\/main\_3 | \UART\_1:BUART:rx\_counter\_load\/q | 3.350 | | Route |  | 1 | \UART\_1:BUART:rx\_counter\_load\ | \UART\_1:BUART:rx\_counter\_load\/q | \UART\_1:BUART:sRX:RxBitCounter\/load | 2.307 | | count7cell | U(3,5) | 1 | \UART\_1:BUART:sRX:RxBitCounter\ |  | SETUP | 5.360 | | Clock |  |  |  |  | Skew | 0.000 | | | | | | |
| \UART\_1:BUART:sRX:RxShifter:u0\/f0\_blk\_stat\_comb | \UART\_1:BUART:sRX:RxSts\/status\_4 | 60.208 MHz | 16.609 | 2150.058 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | datapathcell3 | U(3,5) | 1 | \UART\_1:BUART:sRX:RxShifter:u0\ | \UART\_1:BUART:sRX:RxShifter:u0\/clock | \UART\_1:BUART:sRX:RxShifter:u0\/f0\_blk\_stat\_comb | 3.580 | | Route |  | 1 | \UART\_1:BUART:rx\_fifofull\ | \UART\_1:BUART:sRX:RxShifter:u0\/f0\_blk\_stat\_comb | \UART\_1:BUART:rx\_status\_4\/main\_1 | 3.659 | | macrocell7 | U(3,3) | 1 | \UART\_1:BUART:rx\_status\_4\ | \UART\_1:BUART:rx\_status\_4\/main\_1 | \UART\_1:BUART:rx\_status\_4\/q | 3.350 | | Route |  | 1 | \UART\_1:BUART:rx\_status\_4\ | \UART\_1:BUART:rx\_status\_4\/q | \UART\_1:BUART:sRX:RxSts\/status\_4 | 5.520 | | statusicell2 | U(3,3) | 1 | \UART\_1:BUART:sRX:RxSts\ |  | SETUP | 0.500 | | Clock |  |  |  |  | Skew | 0.000 | | | | | | |
| \UART\_1:BUART:tx\_ctrl\_mark\_last\/q | \UART\_1:BUART:sRX:RxBitCounter\/load | 61.110 MHz | 16.364 | 2150.303 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | macrocell15 | U(3,5) | 1 | \UART\_1:BUART:tx\_ctrl\_mark\_last\ | \UART\_1:BUART:tx\_ctrl\_mark\_last\/clock\_0 | \UART\_1:BUART:tx\_ctrl\_mark\_last\/q | 1.250 | | Route |  | 1 | \UART\_1:BUART:tx\_ctrl\_mark\_last\ | \UART\_1:BUART:tx\_ctrl\_mark\_last\/q | \UART\_1:BUART:rx\_counter\_load\/main\_0 | 4.097 | | macrocell5 | U(3,5) | 1 | \UART\_1:BUART:rx\_counter\_load\ | \UART\_1:BUART:rx\_counter\_load\/main\_0 | \UART\_1:BUART:rx\_counter\_load\/q | 3.350 | | Route |  | 1 | \UART\_1:BUART:rx\_counter\_load\ | \UART\_1:BUART:rx\_counter\_load\/q | \UART\_1:BUART:sRX:RxBitCounter\/load | 2.307 | | count7cell | U(3,5) | 1 | \UART\_1:BUART:sRX:RxBitCounter\ |  | SETUP | 5.360 | | Clock |  |  |  |  | Skew | 0.000 | | | | | | |
| \UART\_1:BUART:pollcount\_0\/q | \UART\_1:BUART:sRX:RxShifter:u0\/route\_si | 61.489 MHz | 16.263 | 2150.404 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | macrocell23 | U(3,3) | 1 | \UART\_1:BUART:pollcount\_0\ | \UART\_1:BUART:pollcount\_0\/clock\_0 | \UART\_1:BUART:pollcount\_0\/q | 1.250 | | Route |  | 1 | \UART\_1:BUART:pollcount\_0\ | \UART\_1:BUART:pollcount\_0\/q | \UART\_1:BUART:rx\_postpoll\/main\_2 | 5.884 | | macrocell6 | U(3,5) | 1 | \UART\_1:BUART:rx\_postpoll\ | \UART\_1:BUART:rx\_postpoll\/main\_2 | \UART\_1:BUART:rx\_postpoll\/q | 3.350 | | Route |  | 1 | \UART\_1:BUART:rx\_postpoll\ | \UART\_1:BUART:rx\_postpoll\/q | \UART\_1:BUART:sRX:RxShifter:u0\/route\_si | 2.309 | | datapathcell3 | U(3,5) | 1 | \UART\_1:BUART:sRX:RxShifter:u0\ |  | SETUP | 3.470 | | Clock |  |  |  |  | Skew | 0.000 | | | | | | |
| \UART\_1:BUART:rx\_state\_3\/q | \UART\_1:BUART:sRX:RxBitCounter\/load | 63.452 MHz | 15.760 | 2150.907 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | macrocell18 | U(2,5) | 1 | \UART\_1:BUART:rx\_state\_3\ | \UART\_1:BUART:rx\_state\_3\/clock\_0 | \UART\_1:BUART:rx\_state\_3\/q | 1.250 | | Route |  | 1 | \UART\_1:BUART:rx\_state\_3\ | \UART\_1:BUART:rx\_state\_3\/q | \UART\_1:BUART:rx\_counter\_load\/main\_2 | 3.493 | | macrocell5 | U(3,5) | 1 | \UART\_1:BUART:rx\_counter\_load\ | \UART\_1:BUART:rx\_counter\_load\/main\_2 | \UART\_1:BUART:rx\_counter\_load\/q | 3.350 | | Route |  | 1 | \UART\_1:BUART:rx\_counter\_load\ | \UART\_1:BUART:rx\_counter\_load\/q | \UART\_1:BUART:sRX:RxBitCounter\/load | 2.307 | | count7cell | U(3,5) | 1 | \UART\_1:BUART:sRX:RxBitCounter\ |  | SETUP | 5.360 | | Clock |  |  |  |  | Skew | 0.000 | | | | | | |
| \UART\_1:BUART:sTX:sCLOCK:TxBitClkGen\/ce0\_reg | \UART\_1:BUART:sTX:sCLOCK:TxBitClkGen\/cs\_addr\_0 | 64.251 MHz | 15.564 | 2151.103 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | datapathcell2 | U(2,5) | 1 | \UART\_1:BUART:sTX:sCLOCK:TxBitClkGen\ | \UART\_1:BUART:sTX:sCLOCK:TxBitClkGen\/clock | \UART\_1:BUART:sTX:sCLOCK:TxBitClkGen\/ce0\_reg | 0.190 | | Route |  | 1 | \UART\_1:BUART:tx\_bitclk\_enable\_pre\ | \UART\_1:BUART:sTX:sCLOCK:TxBitClkGen\/ce0\_reg | \UART\_1:BUART:counter\_load\_not\/main\_2 | 3.540 | | macrocell2 | U(2,5) | 1 | \UART\_1:BUART:counter\_load\_not\ | \UART\_1:BUART:counter\_load\_not\/main\_2 | \UART\_1:BUART:counter\_load\_not\/q | 3.350 | | Route |  | 1 | \UART\_1:BUART:counter\_load\_not\ | \UART\_1:BUART:counter\_load\_not\/q | \UART\_1:BUART:sTX:sCLOCK:TxBitClkGen\/cs\_addr\_0 | 2.294 | | datapathcell2 | U(2,5) | 1 | \UART\_1:BUART:sTX:sCLOCK:TxBitClkGen\ |  | SETUP | 6.190 | | Clock |  |  |  |  | Skew | 0.000 | | | | | | |

[**+ Hold Subsection**](#gjdgxs)

[**+ Source Clock : CyBUS\_CLK : Positive edge**](#gjdgxs)

[**+ Destination Clock : UART\_1\_IntClock : Positive edge**](#gjdgxs)

|  |  |  |  |
| --- | --- | --- | --- |
| Source | Destination | Slack (ns) | Violation |
| Rx\_1(0)/fb | \UART\_1:BUART:pollcount\_1\/main\_3 | 7.563 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | iocell2 | P0[0] | 1 | Rx\_1(0) | Rx\_1(0)/in\_clock | Rx\_1(0)/fb | 2.183 | | Route |  | 1 | Net\_188 | Rx\_1(0)/fb | \UART\_1:BUART:pollcount\_1\/main\_3 | 5.380 | | macrocell22 | U(3,4) | 1 | \UART\_1:BUART:pollcount\_1\ |  | HOLD | 0.000 | | Clock |  |  |  |  | Skew | 0.000 | | | | |
| Rx\_1(0)/fb | \UART\_1:BUART:rx\_state\_0\/main\_9 | 7.582 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | iocell2 | P0[0] | 1 | Rx\_1(0) | Rx\_1(0)/in\_clock | Rx\_1(0)/fb | 2.183 | | Route |  | 1 | Net\_188 | Rx\_1(0)/fb | \UART\_1:BUART:rx\_state\_0\/main\_9 | 5.399 | | macrocell16 | U(3,4) | 1 | \UART\_1:BUART:rx\_state\_0\ |  | HOLD | 0.000 | | Clock |  |  |  |  | Skew | 0.000 | | | | |
| Rx\_1(0)/fb | \UART\_1:BUART:rx\_state\_2\/main\_8 | 7.582 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | iocell2 | P0[0] | 1 | Rx\_1(0) | Rx\_1(0)/in\_clock | Rx\_1(0)/fb | 2.183 | | Route |  | 1 | Net\_188 | Rx\_1(0)/fb | \UART\_1:BUART:rx\_state\_2\/main\_8 | 5.399 | | macrocell19 | U(3,4) | 1 | \UART\_1:BUART:rx\_state\_2\ |  | HOLD | 0.000 | | Clock |  |  |  |  | Skew | 0.000 | | | | |
| Rx\_1(0)/fb | \UART\_1:BUART:pollcount\_0\/main\_2 | 8.218 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | iocell2 | P0[0] | 1 | Rx\_1(0) | Rx\_1(0)/in\_clock | Rx\_1(0)/fb | 2.183 | | Route |  | 1 | Net\_188 | Rx\_1(0)/fb | \UART\_1:BUART:pollcount\_0\/main\_2 | 6.035 | | macrocell23 | U(3,3) | 1 | \UART\_1:BUART:pollcount\_0\ |  | HOLD | 0.000 | | Clock |  |  |  |  | Skew | 0.000 | | | | |
| Rx\_1(0)/fb | \UART\_1:BUART:rx\_status\_3\/main\_6 | 8.218 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | iocell2 | P0[0] | 1 | Rx\_1(0) | Rx\_1(0)/in\_clock | Rx\_1(0)/fb | 2.183 | | Route |  | 1 | Net\_188 | Rx\_1(0)/fb | \UART\_1:BUART:rx\_status\_3\/main\_6 | 6.035 | | macrocell24 | U(3,3) | 1 | \UART\_1:BUART:rx\_status\_3\ |  | HOLD | 0.000 | | Clock |  |  |  |  | Skew | 0.000 | | | | |
| Rx\_1(0)/fb | \UART\_1:BUART:rx\_last\/main\_0 | 8.218 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | iocell2 | P0[0] | 1 | Rx\_1(0) | Rx\_1(0)/in\_clock | Rx\_1(0)/fb | 2.183 | | Route |  | 1 | Net\_188 | Rx\_1(0)/fb | \UART\_1:BUART:rx\_last\/main\_0 | 6.035 | | macrocell25 | U(3,3) | 1 | \UART\_1:BUART:rx\_last\ |  | HOLD | 0.000 | | Clock |  |  |  |  | Skew | 0.000 | | | | |
| Rx\_1(0)/fb | \UART\_1:BUART:sRX:RxShifter:u0\/route\_si | 14.138 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | iocell2 | P0[0] | 1 | Rx\_1(0) | Rx\_1(0)/in\_clock | Rx\_1(0)/fb | 2.183 | | Route |  | 1 | Net\_188 | Rx\_1(0)/fb | \UART\_1:BUART:rx\_postpoll\/main\_1 | 6.296 | | macrocell6 | U(3,5) | 1 | \UART\_1:BUART:rx\_postpoll\ | \UART\_1:BUART:rx\_postpoll\/main\_1 | \UART\_1:BUART:rx\_postpoll\/q | 3.350 | | Route |  | 1 | \UART\_1:BUART:rx\_postpoll\ | \UART\_1:BUART:rx\_postpoll\/q | \UART\_1:BUART:sRX:RxShifter:u0\/route\_si | 2.309 | | datapathcell3 | U(3,5) | 1 | \UART\_1:BUART:sRX:RxShifter:u0\ |  | HOLD | 0.000 | | Clock |  |  |  |  | Skew | 0.000 | | | | |

[**+ Source Clock : UART\_1\_IntClock : Positive edge**](#gjdgxs)

[**+ Destination Clock : UART\_1\_IntClock : Positive edge**](#gjdgxs)

|  |  |  |  |
| --- | --- | --- | --- |
| Source | Destination | Slack (ns) | Violation |
| \UART\_1:BUART:rx\_status\_3\/q | \UART\_1:BUART:sRX:RxSts\/status\_3 | 1.585 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | macrocell24 | U(3,3) | 1 | \UART\_1:BUART:rx\_status\_3\ | \UART\_1:BUART:rx\_status\_3\/clock\_0 | \UART\_1:BUART:rx\_status\_3\/q | 1.250 | | Route |  | 1 | \UART\_1:BUART:rx\_status\_3\ | \UART\_1:BUART:rx\_status\_3\/q | \UART\_1:BUART:sRX:RxSts\/status\_3 | 2.335 | | statusicell2 | U(3,3) | 1 | \UART\_1:BUART:sRX:RxSts\ |  | HOLD | -2.000 | | Clock |  |  |  |  | Skew | 0.000 | | | | |
| \UART\_1:BUART:sRX:RxBitCounter\/count\_0 | \UART\_1:BUART:rx\_bitclk\_enable\/main\_2 | 2.946 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | count7cell | U(3,5) | 1 | \UART\_1:BUART:sRX:RxBitCounter\ | \UART\_1:BUART:sRX:RxBitCounter\/clock | \UART\_1:BUART:sRX:RxBitCounter\/count\_0 | 0.620 | | Route |  | 1 | \UART\_1:BUART:rx\_count\_0\ | \UART\_1:BUART:sRX:RxBitCounter\/count\_0 | \UART\_1:BUART:rx\_bitclk\_enable\/main\_2 | 2.326 | | macrocell20 | U(3,5) | 1 | \UART\_1:BUART:rx\_bitclk\_enable\ |  | HOLD | 0.000 | | Clock |  |  |  |  | Skew | 0.000 | | | | |
| \UART\_1:BUART:sRX:RxBitCounter\/count\_4 | \UART\_1:BUART:rx\_state\_3\/main\_7 | 2.947 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | count7cell | U(3,5) | 1 | \UART\_1:BUART:sRX:RxBitCounter\ | \UART\_1:BUART:sRX:RxBitCounter\/clock | \UART\_1:BUART:sRX:RxBitCounter\/count\_4 | 0.620 | | Route |  | 1 | \UART\_1:BUART:rx\_count\_4\ | \UART\_1:BUART:sRX:RxBitCounter\/count\_4 | \UART\_1:BUART:rx\_state\_3\/main\_7 | 2.327 | | macrocell18 | U(2,5) | 1 | \UART\_1:BUART:rx\_state\_3\ |  | HOLD | 0.000 | | Clock |  |  |  |  | Skew | 0.000 | | | | |
| \UART\_1:BUART:sRX:RxBitCounter\/count\_6 | \UART\_1:BUART:rx\_state\_3\/main\_5 | 2.951 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | count7cell | U(3,5) | 1 | \UART\_1:BUART:sRX:RxBitCounter\ | \UART\_1:BUART:sRX:RxBitCounter\/clock | \UART\_1:BUART:sRX:RxBitCounter\/count\_6 | 0.620 | | Route |  | 1 | \UART\_1:BUART:rx\_count\_6\ | \UART\_1:BUART:sRX:RxBitCounter\/count\_6 | \UART\_1:BUART:rx\_state\_3\/main\_5 | 2.331 | | macrocell18 | U(2,5) | 1 | \UART\_1:BUART:rx\_state\_3\ |  | HOLD | 0.000 | | Clock |  |  |  |  | Skew | 0.000 | | | | |
| \UART\_1:BUART:sTX:sCLOCK:TxBitClkGen\/ce1\_reg | \UART\_1:BUART:tx\_state\_1\/main\_4 | 3.111 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | datapathcell2 | U(2,5) | 1 | \UART\_1:BUART:sTX:sCLOCK:TxBitClkGen\ | \UART\_1:BUART:sTX:sCLOCK:TxBitClkGen\/clock | \UART\_1:BUART:sTX:sCLOCK:TxBitClkGen\/ce1\_reg | 0.190 | | Route |  | 1 | \UART\_1:BUART:tx\_counter\_dp\ | \UART\_1:BUART:sTX:sCLOCK:TxBitClkGen\/ce1\_reg | \UART\_1:BUART:tx\_state\_1\/main\_4 | 2.921 | | macrocell11 | U(2,4) | 1 | \UART\_1:BUART:tx\_state\_1\ |  | HOLD | 0.000 | | Clock |  |  |  |  | Skew | 0.000 | | | | |
| \UART\_1:BUART:sRX:RxBitCounter\/count\_2 | \UART\_1:BUART:rx\_bitclk\_enable\/main\_0 | 3.253 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | count7cell | U(3,5) | 1 | \UART\_1:BUART:sRX:RxBitCounter\ | \UART\_1:BUART:sRX:RxBitCounter\/clock | \UART\_1:BUART:sRX:RxBitCounter\/count\_2 | 0.620 | | Route |  | 1 | \UART\_1:BUART:rx\_count\_2\ | \UART\_1:BUART:sRX:RxBitCounter\/count\_2 | \UART\_1:BUART:rx\_bitclk\_enable\/main\_0 | 2.633 | | macrocell20 | U(3,5) | 1 | \UART\_1:BUART:rx\_bitclk\_enable\ |  | HOLD | 0.000 | | Clock |  |  |  |  | Skew | 0.000 | | | | |
| \UART\_1:BUART:sRX:RxBitCounter\/count\_1 | \UART\_1:BUART:rx\_bitclk\_enable\/main\_1 | 3.259 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | count7cell | U(3,5) | 1 | \UART\_1:BUART:sRX:RxBitCounter\ | \UART\_1:BUART:sRX:RxBitCounter\/clock | \UART\_1:BUART:sRX:RxBitCounter\/count\_1 | 0.620 | | Route |  | 1 | \UART\_1:BUART:rx\_count\_1\ | \UART\_1:BUART:sRX:RxBitCounter\/count\_1 | \UART\_1:BUART:rx\_bitclk\_enable\/main\_1 | 2.639 | | macrocell20 | U(3,5) | 1 | \UART\_1:BUART:rx\_bitclk\_enable\ |  | HOLD | 0.000 | | Clock |  |  |  |  | Skew | 0.000 | | | | |
| \UART\_1:BUART:sRX:RxBitCounter\/count\_5 | \UART\_1:BUART:rx\_state\_3\/main\_6 | 3.262 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | count7cell | U(3,5) | 1 | \UART\_1:BUART:sRX:RxBitCounter\ | \UART\_1:BUART:sRX:RxBitCounter\/clock | \UART\_1:BUART:sRX:RxBitCounter\/count\_5 | 0.620 | | Route |  | 1 | \UART\_1:BUART:rx\_count\_5\ | \UART\_1:BUART:sRX:RxBitCounter\/count\_5 | \UART\_1:BUART:rx\_state\_3\/main\_6 | 2.642 | | macrocell18 | U(2,5) | 1 | \UART\_1:BUART:rx\_state\_3\ |  | HOLD | 0.000 | | Clock |  |  |  |  | Skew | 0.000 | | | | |
| \UART\_1:BUART:rx\_state\_0\/q | \UART\_1:BUART:rx\_state\_0\/main\_1 | 3.571 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | macrocell16 | U(3,4) | 1 | \UART\_1:BUART:rx\_state\_0\ | \UART\_1:BUART:rx\_state\_0\/clock\_0 | \UART\_1:BUART:rx\_state\_0\/q | 1.250 | | macrocell16 | U(3,4) | 1 | \UART\_1:BUART:rx\_state\_0\ | \UART\_1:BUART:rx\_state\_0\/q | \UART\_1:BUART:rx\_state\_0\/main\_1 | 2.321 | | macrocell16 | U(3,4) | 1 | \UART\_1:BUART:rx\_state\_0\ |  | HOLD | 0.000 | | Clock |  |  |  |  | Skew | 0.000 | | | | |
| \UART\_1:BUART:rx\_state\_0\/q | \UART\_1:BUART:rx\_state\_2\/main\_1 | 3.571 |  |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | macrocell16 | U(3,4) | 1 | \UART\_1:BUART:rx\_state\_0\ | \UART\_1:BUART:rx\_state\_0\/clock\_0 | \UART\_1:BUART:rx\_state\_0\/q | 1.250 | | Route |  | 1 | \UART\_1:BUART:rx\_state\_0\ | \UART\_1:BUART:rx\_state\_0\/q | \UART\_1:BUART:rx\_state\_2\/main\_1 | 2.321 | | macrocell19 | U(3,4) | 1 | \UART\_1:BUART:rx\_state\_2\ |  | HOLD | 0.000 | | Clock |  |  |  |  | Skew | 0.000 | | | | |

[**+ Clock To Output Section**](#gjdgxs)

[**+ UART\_1\_IntClock**](#gjdgxs)

|  |  |  |
| --- | --- | --- |
| Source | Destination | Delay (ns) |
| \UART\_1:BUART:txn\/q | Tx\_1(0)\_PAD | 29.740 |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | Type | Location | Fanout | Instance/Net | Source | Dest | Delay (ns) | | macrocell10 | U(2,3) | 1 | \UART\_1:BUART:txn\ | \UART\_1:BUART:txn\/clock\_0 | \UART\_1:BUART:txn\/q | 1.250 | | Route |  | 1 | \UART\_1:BUART:txn\ | \UART\_1:BUART:txn\/q | Net\_183/main\_0 | 2.609 | | macrocell1 | U(2,3) | 1 | Net\_183 | Net\_183/main\_0 | Net\_183/q | 3.350 | | Route |  | 1 | Net\_183 | Net\_183/q | Tx\_1(0)/pin\_input | 6.335 | | iocell3 | P12[3] | 1 | Tx\_1(0) | Tx\_1(0)/pin\_input | Tx\_1(0)/pad\_out | 16.196 | | Route |  | 1 | Tx\_1(0)\_PAD | Tx\_1(0)/pad\_out | Tx\_1(0)\_PAD | 0.000 | | Clock |  |  |  |  | Clock path delay | 0.000 | | | |